WHAT IS CLAIMED IS:

1. A method comprising:

determining latencies of transactions on a bus, each latency representing a time period from a first event of a corresponding transaction to a second event of said corresponding transaction; and

selecting a first retry latency for a first transaction from a plurality of retry latencies responsive to latencies of N previous transactions, wherein N is a positive integer, said first retry latency indicative of a point in time, measured from said first event of said first transaction on said bus, that said first transaction is retried on said bus if said second event of said first transaction does not occur before said point in time.

2. The method as recited in claim 1 further comprising:

replacing one of said latencies of said N previous transactions with a first latency of said first transaction; and

selecting a second retry latency of said plurality of retry latencies for a second transaction responsive to said latencies of N previous transactions subsequent to said replacing.

3. The method as recited in claim 2 wherein said one of said latencies of N previous transactions corresponds to a least recent transaction of said previous transactions.

4. The method as recited in claim 1 wherein said selecting comprises selecting a minimum retry latency of said plurality of retry latencies responsive to at least a first

number of said latencies of N previous transactions being latencies greater than a maximum retry latency of said plurality of retry latencies.

5. The method as recited in claim 1 wherein said selecting comprises selecting a maximum retry latency of said plurality of retry latencies responsive to: (i) a currently selected retry latency being other than a minimum retry latency of said plurality of retry latencies; and (ii) at least a first number of said latencies of N previous transactions being latencies less than said maximum retry latency and greater than said currently selected retry latency.

6. The method as recited in claim 1 wherein said selecting said first retry latency is responsive to: (i) a currently selected retry latency being a minimum retry latency of said plurality of retry latencies; and (ii) at least a first number of said latencies of N previous transactions being latencies less than said first retry latency.

7. The method as recited in claim 6 wherein said first retry latency is not a maximum retry latency of said plurality of retry latencies.

8. The method as recited in claim 1 wherein said plurality of retry latencies includes a minimum retry latency, a maximum retry latency, and a nominal retry latency.

9. The method as recited in claim 8 further comprising initially selecting said nominal retry latency.

10. The method as recited in claim 8 further comprising changing from said nominal retry latency to said minimum retry latency responsive to at least a first number of said latencies of N previous transactions being latencies greater than said maximum retry latency.

11. The method as recited in claim 8 further comprising changing from said nominal retry latency to said maximum retry latency responsive to at least a first number of said latencies of N previous transactions being latencies greater than said nominal retry latency and less than said maximum retry latency.

12. The method as recited in claim 8 further comprising changing from said maximum retry latency to said minimum retry latency responsive to at least a first number of said latencies of N previous transactions being latencies greater than said maximum retry latency.

13. The method as recited in claim 8 further comprising changing from said minimum retry latency to said nominal retry latency responsive to at least a first number of said latencies of N previous transactions being latencies greater than said minimum retry latency and less than said nominal retry latency.

14. The method as recited in claim 1 further comprising retrying said first transaction at said point in time if said second event does not occur before said point in time.

15. The method as recited in claim 1 wherein said first retry latency is a number of clock cycle of a bus clock corresponding to said bus.

16. The method as recited in claim 1 wherein said selecting is performed by a target of said first transaction.

17. The method as recited in claim 16 wherein said determining is performed by said target, and wherein said transactions are transactions targeting said target.

18. The method as recited in claim 1 wherein said first event is a beginning of said corresponding transaction and wherein said second event is a first data transfer of said

corresponding transaction.

19. The method as recited in claim 1 wherein said first event is a previous data transfer of said corresponding transaction and said second event is a subsequent data transfer of said corresponding transaction.

20. The method as recited in claim 1 wherein said determining comprises measuring said latencies.

21. The method as recited in claim 1 wherein said determining comprises calculating said latencies from multiple internal states of a system including said bus.

22. The method as recited in claim 21 wherein said multiple internal states include a memory read latency, a number of transactions queue in a memory controller, and an amount of traffic on a system bus to which said memory controller is coupled.

23. An apparatus comprising:

a buffer configured to store latencies of transactions on a bus, each of said latencies representing a period of time from a first event of a corresponding transaction to a second event of said corresponding transaction; and

a circuit configured to select a first retry latency for a first transaction from a plurality of retry latencies responsive to latencies of N previous transactions, wherein N is a positive integer, said first retry latency indicative of a point in time, measured from said first event of said first transaction on said bus, that said first transaction is retried on said bus if said second event of said first transaction does not occur before said point

in time.

24. The apparatus as recited in claim 23 wherein said circuit is further configured to replace one of said latencies stored in said buffer with a first latency of said first transaction, and wherein said circuit is further configured to select a second retry latency of said plurality of retry latencies for a second transaction responsive to said latencies of N previous transactions subsequent to said replacing.

25. The apparatus as recited in claim 24 wherein said buffer is a first-in, first-out buffer, and wherein one of said latencies corresponds to a least recent transaction of said previous transactions.

26. The apparatus as recited in claim 23 wherein said first retry latency is a minimum retry latency of said plurality of retry latencies responsive to at least a first number of said latencies stored in said buffer being latencies greater than a maximum retry latency of said plurality of retry latencies.

27. The apparatus as recited in claim 23 wherein said first retry latency is a maximum retry latency of said plurality of retry latencies responsive to: (i) a currently selected retry latency being other than a minimum retry latency of said plurality of retry latencies; and (ii) at least a first number of said latencies stored in said buffer being latencies less than said maximum retry latency and greater than said currently selected retry latency.

28. The apparatus as recited in claim 23 wherein said circuit is configured to select said first retry latency responsive to: (i) a currently selected retry latency being a minimum retry latency of said plurality of retry latencies; and (ii) at least a first number of said latencies stored in said buffer being latencies less than said first retry latency.

29. The apparatus as recited in claim 28 wherein said first retry latency is not a maximum

retry latency of said plurality of retry latencies.

30. The apparatus as recited in claim 23 wherein said plurality of retry latencies includes a minimum retry latency, a maximum retry latency, and a nominal retry latency.

31. The apparatus as recited in claim 30 wherein said circuit is further configured to initially select said nominal retry latency.

32. The apparatus as recited in claim 30 wherein said circuit is further configured to change from said nominal retry latency to said minimum retry latency responsive to at least a first number of said latencies of N previous transactions being latencies greater than said maximum retry latency.

33. The apparatus as recited in claim 30 wherein said circuit is further configured to change from said nominal retry latency to said maximum retry latency responsive to at least a first number of said latencies of N previous transactions being latencies greater than said nominal retry latency and less than said maximum retry latency.

34. The apparatus as recited in claim 30 wherein said circuit is further configured to change from said maximum retry latency to said minimum retry latency responsive to at least a first number of said latencies of N previous transactions being latencies greater than said maximum retry latency.

35. The apparatus as recited in claim 30 wherein said circuit is further configured to change from said minimum retry latency to said nominal retry latency responsive to at least a first number of said latencies of N previous transactions being latencies greater than said minimum retry latency and less than said nominal retry latency.

36. The apparatus as recited in claim 23 further comprising a second circuit coupled to

said first circuit, said second circuit configured to retry said first transaction at said point in time if said second event does not occur before said point in time.

37. The apparatus as recited in claim 23 wherein said first retry latency is a number of clock cycle of a bus clock corresponding to said bus.

38. The apparatus as recited in claim 23 wherein said circuit is included in a target of said first transaction.

39. The apparatus as recited in claim 38 wherein said target of said transaction is configured to measure said latencies of said transactions, and wherein said transactions are transactions targeting said target.

40. The apparatus as recited in claim 38 wherein said target of said transaction is configured to calculate said latencies from multiple internal states of a system including said apparatus.

41. The apparatus as recited in claim 40 wherein said multiple internal states include a memory read latency, a number of transactions queue in a memory controller, and an amount of traffic on a system bus to which said memory controller is coupled.

42. The apparatus as recited in claim 23 wherein said first event is a beginning of said corresponding transaction and wherein said second event is a first data transfer of said corresponding transaction.

43. The apparatus as recited in claim 23 wherein said first event is a previous data transfer of said corresponding transaction and said second event is a subsequent data transfer of said corresponding transaction.